TUNABLE VARIABLE RESISTANCE MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application, filed under 35 U.S.C. §119, is a continuation-in-part from and claims the benefit of U.S. patent application Ser. No. 14/727,618 filed on Jun. 1, 2015, and entitled "Tunable Variable Resistance Memory Device," the contents of which are hereby incorporated by reference in their entirety.

FIELD OF THE DISCLOSURE

[0002] The present disclosure is generally related to tunable variable resistance memory devices, and more particularly to tunable ion-conduction variable resistance memory devices.

BACKGROUND

[0003] A typical variable resistance memory device, or memristor, may be "programmed" to have two logic states, such as a low resistance state (on-state) and a high resistance state (off-state). In order to program the memristor into a low resistance state, a potential difference may be applied across a memory stack of the memristor. The potential difference may form one or more conductive pathways through the memory device, thereby decreasing the resistance of the memristor. In order to program the memristor into a high resistance state, a reverse potential difference may be applied across the memory stack. The reverse potential difference may alter, eliminate, or reduce the one or more conductive pathways, increasing the resistance of the memristor. The programmed resistance may be permanent, or semi-permanent, until changed by another applied potential. To read the resistance state of the memristor, a smaller potential difference (e.g., a voltage that is insufficient to change the resistance state) may be applied to the memory stack and a resultant current may be measured to determine the resistance state.

[0004] U.S. Pat. No. 7,087,919, filed on Apr. 7, 2004 and entitled, "Layered Resistance Variable Memory Device and Method of Fabrication," describes an example of a variable resistance memory device that relies on ion conduction to alter a resistance of the device. The device has at least one layer of silver-selenide between a first chalcogenide glass layer and a conductive adhesion layer, which may also be a chalcogenide glass layer. When a potential difference is placed across the device, the silver may form one or more conductive channels through the chalcogenide glass layer, thereby altering a resistance of the device. U.S. Pat. No. 7,087,919 is hereby incorporated by reference in its entirety.

[0005] U.S. Pat. No. 7,190,048, filed on Jul. 19, 2004 and entitled "Resistance Variable Memory Device and Method of Fabrication," describes another example of a variable resistance memory device that includes a stack with at least one layer of tin-chalcogenide proximate a first chalcogenide glass layer. During a conditioning step, tin-selenide from the tin-chalcogenide layer is incorporated into the chalcogenide glass layer to form conducting channels. Movement of silver ions into or out of that conducting channel during subsequent programming forms a conductive pathway, which causes a detectable resistance change across the memory device. U.S. Pat. No. 7,190,048 is hereby incorporated by reference in its entirety.

[0006] One potential challenge associated with typical memristor devices is that when the memristor is in a low resistance state, a high current may be drawn through the memristor in response to an applied voltage potential. The high current may result in high power consumption, which may decrease the economic value, or feasibility, of using typical memristor devices for some applications such as high density arrays. The high current may also produce heat that may alter the chemical structure of the device stack. Another potential problem associated with typical memristors is that the dynamic range of programmable resistance may be limited. For example, the dynamic range of programmable resistance of a typical memristor may only enable binary resistance states (e.g., an on-state or an off-state). As such, typical memristors may not be suitable for applications that depend on multiple discrete states or a continuous range of states.

SUMMARY

[0007] Accordingly, the present disclosure sets forth a variable resistance memory device that substantially solves, reduces, or eliminates at least one of the above-noted drawbacks of existing devices.

[0008] In an embodiment, a variable resistance memory device includes a first electrode and a second electrode. The device further includes a chalcogenide glass layer between the first electrode and the second electrode. The chalcogenide glass layer includes a chalcogenide glass material co-deposited with a metal material. The device also includes a metal ion source structure between the chalcogenide glass layer and the second electrode. The device includes a buffer layer between the first electrode and the chalcogenide glass layer.

[0009] In an embodiment, the metal material may include chromium, tungsten, copper, cobalt, indium, or a combination thereof. The chalcogenide glass material may include germanium selenide. The buffer layer may include the chalcogenide glass material and may exclude the metal material.

[0010] In an embodiment, the metal ion source structure may include a first adhesion layer and a second adhesion layer. The metal ion source structure may further include a mobile metal layer between the first adhesion layer and the second adhesion layer. The first adhesion layer and the second adhesion layer may include the chalcogenide glass material. The metal layer may include silver. A thickness of the metal layer may be between 600 Å and 1000 Å. A thickness of the first adhesion layer and the second adhesion layer may be less than 200 Å.

[0011] In an embodiment, the device further includes a metal-chalcogenide layer between the chalcogenide glass layer and the metal ion source structure. The metal chalcogenide layer may include tin-selenide. A thickness of the metal chalcogenide layer may be between 750 Å and 1250 Å. A thickness of the chalcogenide glass layer may be between 250 Å and 350 Å. A thickness of the buffer layer may be between 50 Å and 150 Å.

[0012] In an embodiment, the device further includes another buffer layer between the chalcogenide glass layer and the metal ion source structure. Further, an electrical resistance between the first electrode and the second elec-